WHAT IS CLAIMED IS:

1. A cache coherent memory system for use in a non-homogeneous multiprocessor system, comprising:

a first processor;

a first cache associated with said first processor;

one of a second processor or other device non-homogeneous with said first processor; and

multiprocessor bus means connected to said first cache of said first processor and to said one of a second processor or other device non-homogeneous with said first processor for providing cache coherent communications via said bus means.

2. The apparatus of claim 1 comprising, in addition, a second cache associated with said one of a second processor or other device non-homogeneous with said first processor and connected to said bus means.

3. A cache coherent multiprocessor system, comprising:

shared memory;

a first cache;

a first processor that normally communicates directly with said shared memory and stores retrieved data in said first cache;

a second processor, of a configuration different from said first processor, said second processor not typically communicating directly with said shared memory; and

a cache coherent system communicating with both said first and second processors.

4. The apparatus of claim 3 comprising, in addition:

a second cache, associated with said second processor, in which data normally first obtained from shared memory is stored.

5. A method of sharing the use of system memory data by heterogeneous devices in a multiprocessor system, comprising:

sending a request for a copy of system memory stored data to coherent memory configured caches of other devices, including caches of heterogeneous devices, before attempting retrieval directly from system memory;

storing data, retrieved from a cache of a heterogeneous device in a cache associated with the requesting device; and

updating a state table associated with each coherent memory configured cache to reflect the appropriate state after the data is stored in the cache of the requesting device.

6. A method of sharing the use of system memory data by heterogeneous devices in a multiprocessor system, comprising:

sending a request for a copy of system memory stored data to coherent memory configured apparatus of other devices, where at least one of the devices is heterogeneous, before attempting retrieval directly from system memory;

storing data, retrieved from a heterogeneous device, in a cache associated with the requesting device; and

updating a state table associated with each coherent memory configured apparatus to reflect the appropriate state after the data is stored in the cache of the requesting device.

7. A computer program product for sharing the use of system memory data by heterogeneous devices in a multiprocessor system, the computer program product having a medium with a computer program embodied thereon, the computer program

comprising:

computer code for sending a request for a copy of system memory stored data to coherent memory configured caches of other devices, including caches of heterogeneous devices, before attempting retrieval directly from system memory;

computer code for storing data, retrieved from a cache of a heterogeneous device, in a cache associated with the requesting device; and

computer code for updating a state table associated with each coherent memory configured cache to reflect the appropriate state after the data is stored in the cache of the requesting device.

8. A computer program product for sharing the use of system memory data by heterogeneous devices in a multiprocessor system, the computer program product having a medium with a computer program embodied thereon, the computer program comprising:

computer code for sending a request for a copy of system memory stored data to coherent memory configured apparatus of other devices, where at least one of the devices is heterogeneous, before attempting retrieval directly from system memory;

computer code for storing data, retrieved from a heterogeneous device, in a cache associated with the requesting device; and

computer code for updating a state table associated with each coherent memory configured apparatus to reflect the appropriate state after the data is stored in the cache of the requesting device.